



#15/B

15.29/5629 3/13/03

Mullish

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: )  
TSUGANE et al. )  
Serial No. 09/759,666 )  
Filed: January 13, 2001 )  
For: SEMICONDUCTOR DEVICES AND METHODS )  
FOR MANUFACTURING THE SAME )

Group Art Unit: 2813

Examiner: Schillinger, L.

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AMENDMENT

Box RCE  
Commissioner for Patents  
Washington, DC 20231

Dear Sirs:

Applicant has filed an RCE and request for extension of time together with this Amendment in response to the Office Action dated September 3, 2002. Please enter and consider the following.

IN THE CLAIMS:

Please amend claim 16 as follows:

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C.7  
B1

16. (twice amended) A method according to claim 15, further comprising, prior to forming the storage node of the cell capacitor and the lower electrode of the capacitor element, forming an additional conducting layer and etching the additional conducting layer to form a word line that is a component of the DRAM and to form a connection layer that is located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device.